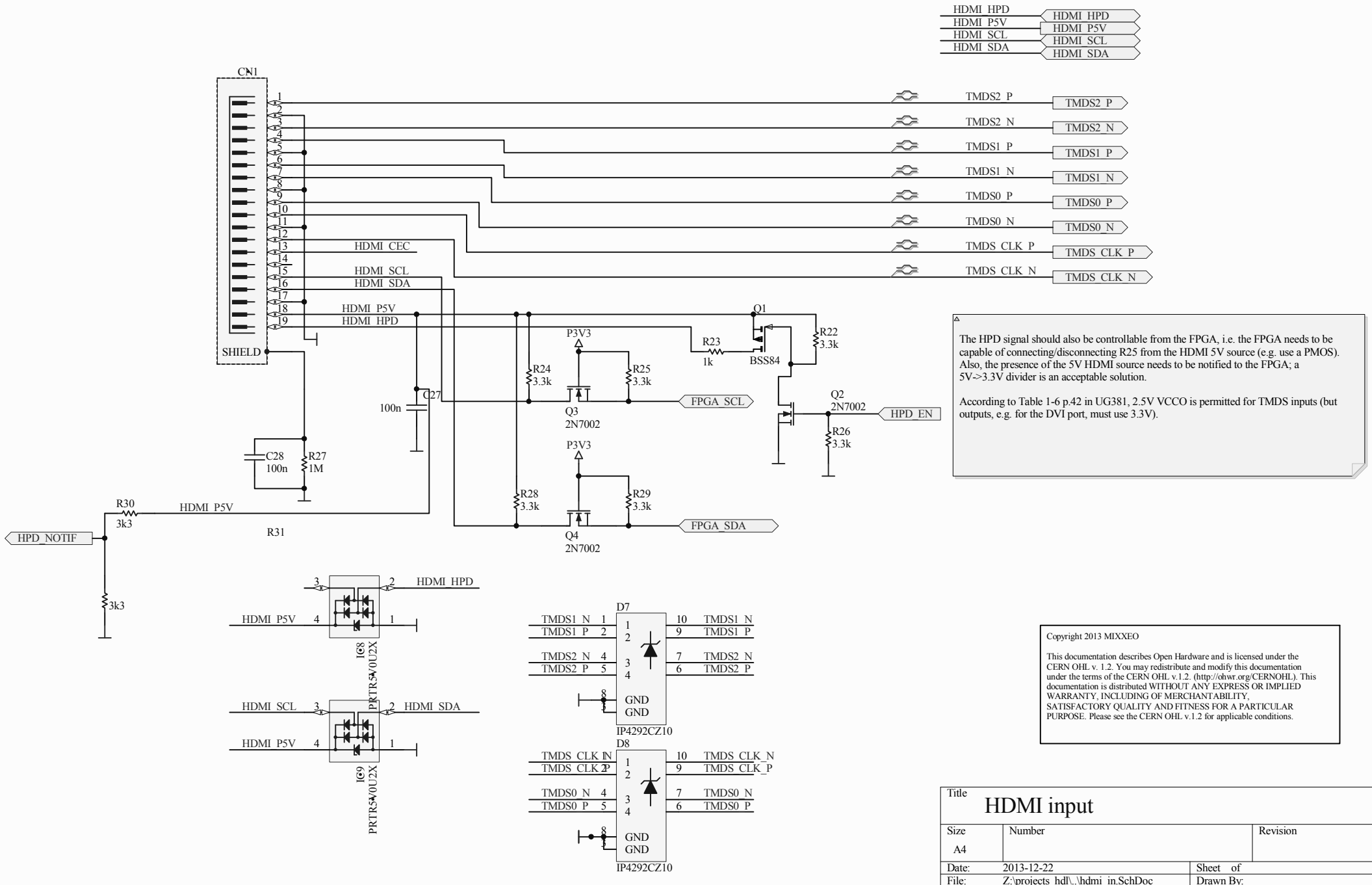
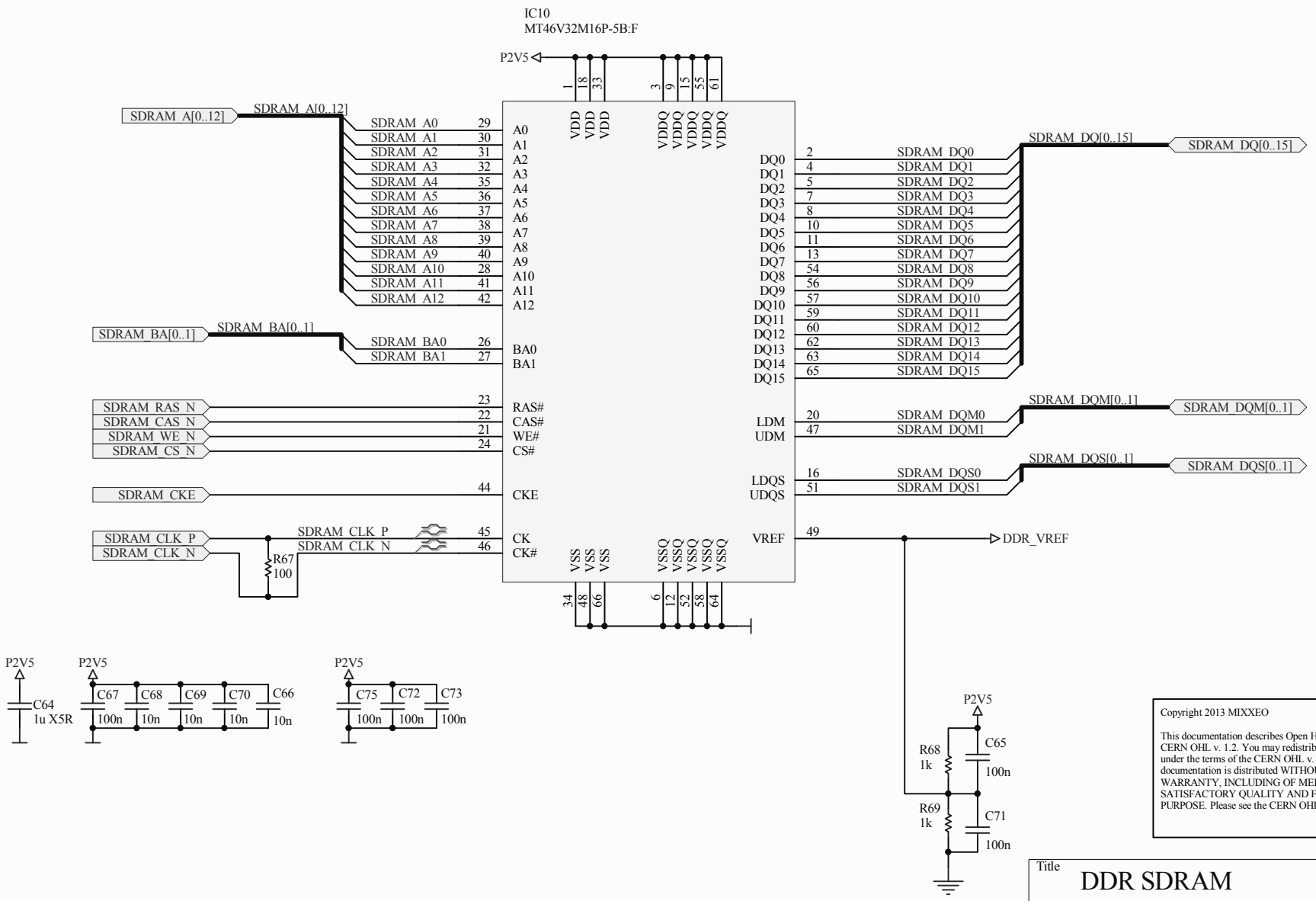


The HPD signal should also be controllable from the FPGA, i.e. the FPGA needs to be capable of connecting/disconnecting R25 from the HDMI 5V source (e.g. use a PMOS). Also, the presence of the 5V HDMI source needs to be notified to the FPGA; a 5V->3.3V divider is an acceptable solution.

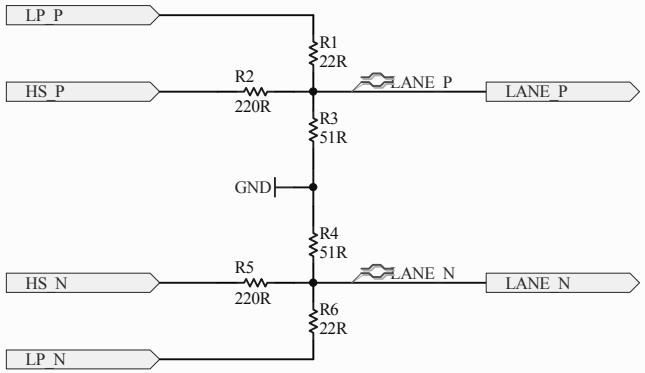
According to Table 1-6 p.42 in UG381, 2.5V VCCO is permitted for TMDS inputs (but outputs, e.g. for the DVI port, must use 3.3V).

Title: HDMI input		
Size: A4	Number:	Revision:
Date: 2013-12-22		Sheet of
File: Z:\projects_hdl\..\hdmi_in.SchDoc		Drawn By:

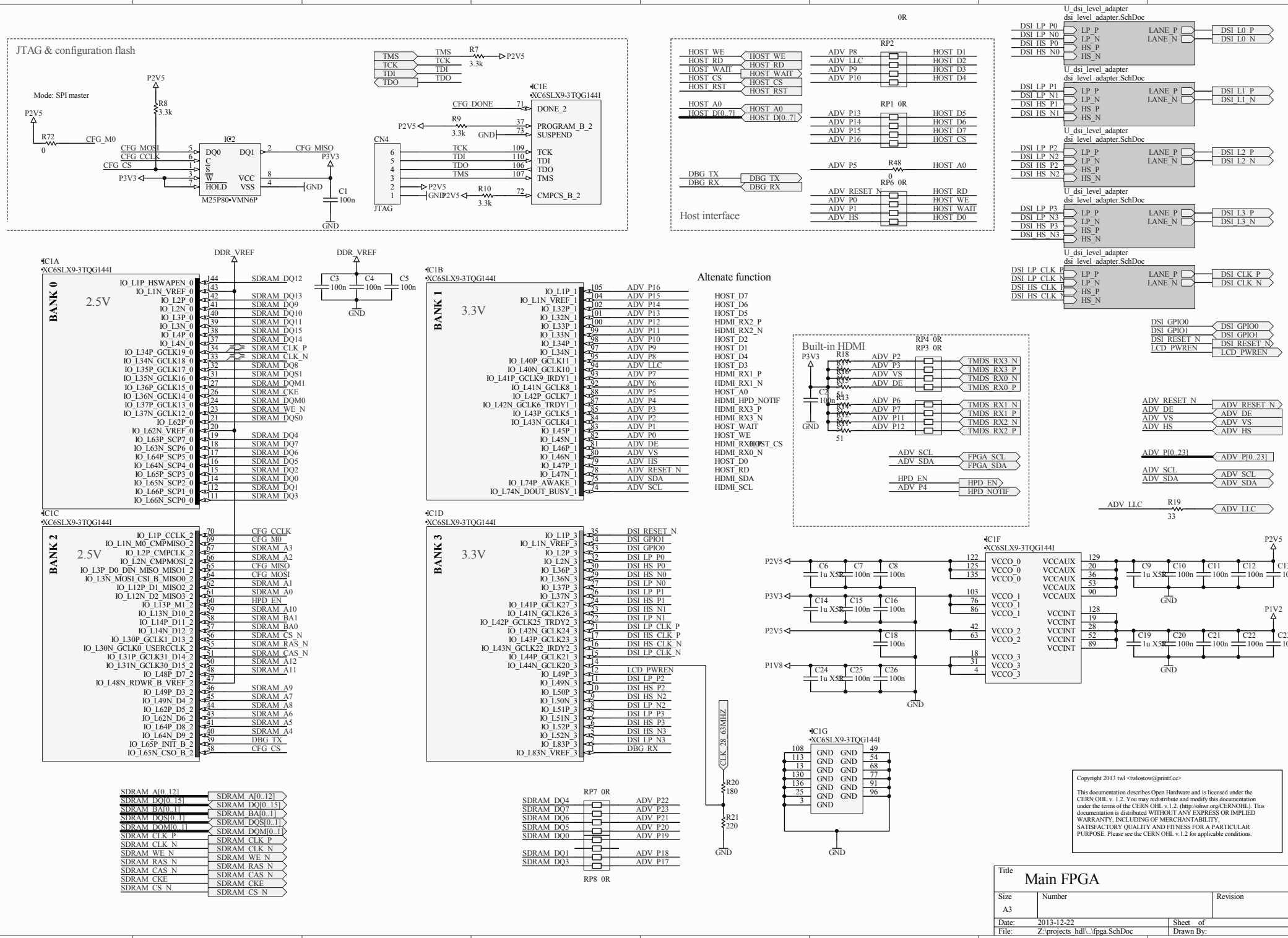


Title	DDR SDRAM	
Size: A4	Number:	Revision:
Date: 2013-12-22		Sheet of
File: Z:\projects_hdl\..\ddr_sdram.SchDoc		Drawn By:

Not matched, place as close as possible to the FPGA pins



Title	SSTL/LVTTL to DSI level adapter	
Size: A4	Number:	Revision:
Date: 2013-12-22		Sheet of
File: Z:\projects_hdl\..\dsi_level_adapter.SchDoc		Drawn By:


JTAG & configuration flash
Mode: SPI master
M25P80-VMN6P
JTAG
Host interface
Built-in HDMI
Alternate function
HOST_D7
HOST_D6
HOST_D5
HDMI_RX2_P
HDMI_RX2_N
HOST_D2
HOST_D1
HOST_D4
HOST_D3
HDMI_RX1_P
HDMI_RX1_N
HOST_A0
HDMI_HPD_NOTIF
HDMI_RX3_P
HDMI_RX3_N
HOST_WAIT
HOST_WE
HDMI_RX0_P
HOST_CS
HDMI_RX0_N
HOST_D0
HOST_RD
HDMI_SDA
HDMI_SCL
BANK 0
2.5V
BANK 1
3.3V
BANK 2
2.5V
BANK 3
3.3V
DDR_VREF
U_dsi_level_adapter
dsi_level_adapter.SchDoc
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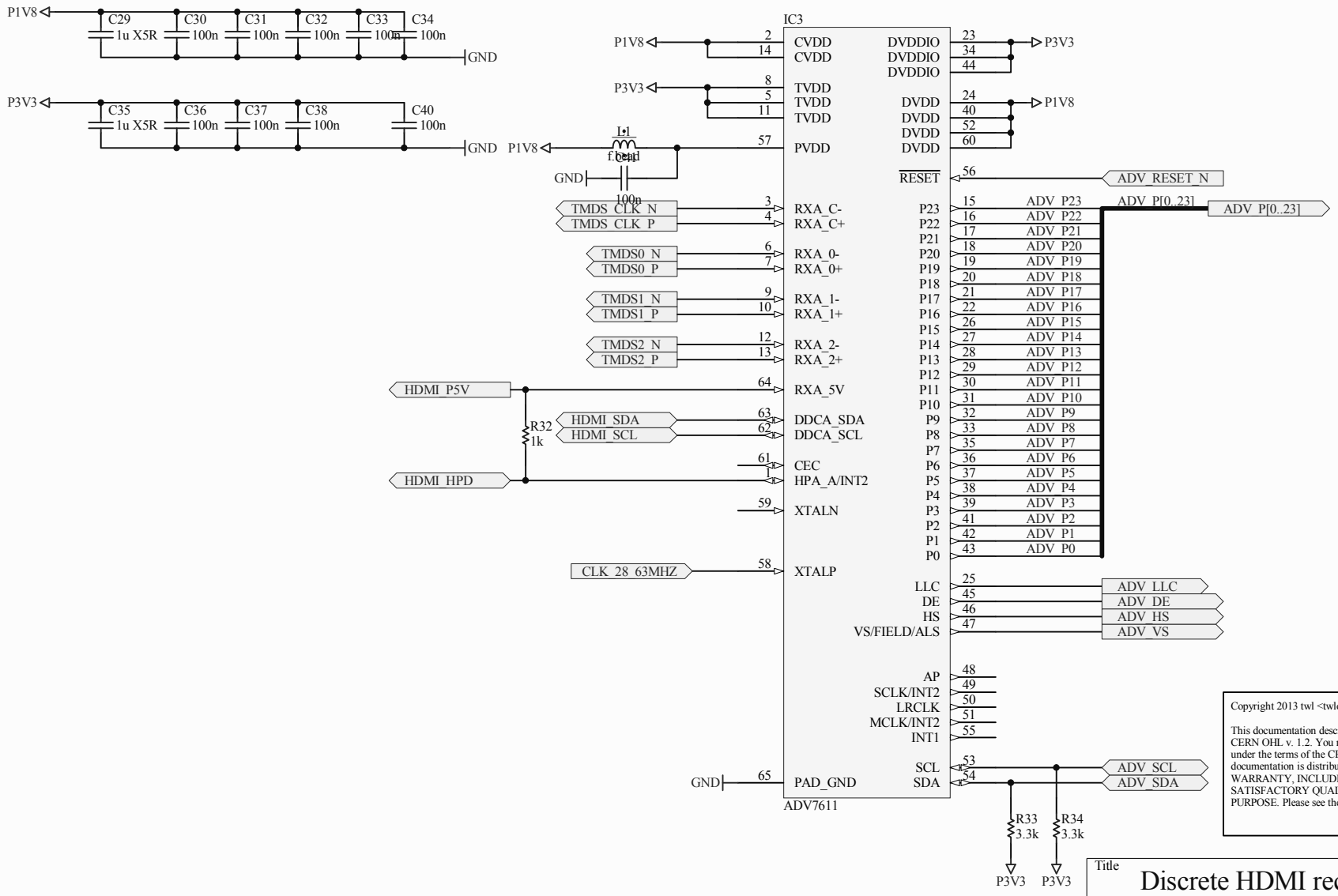
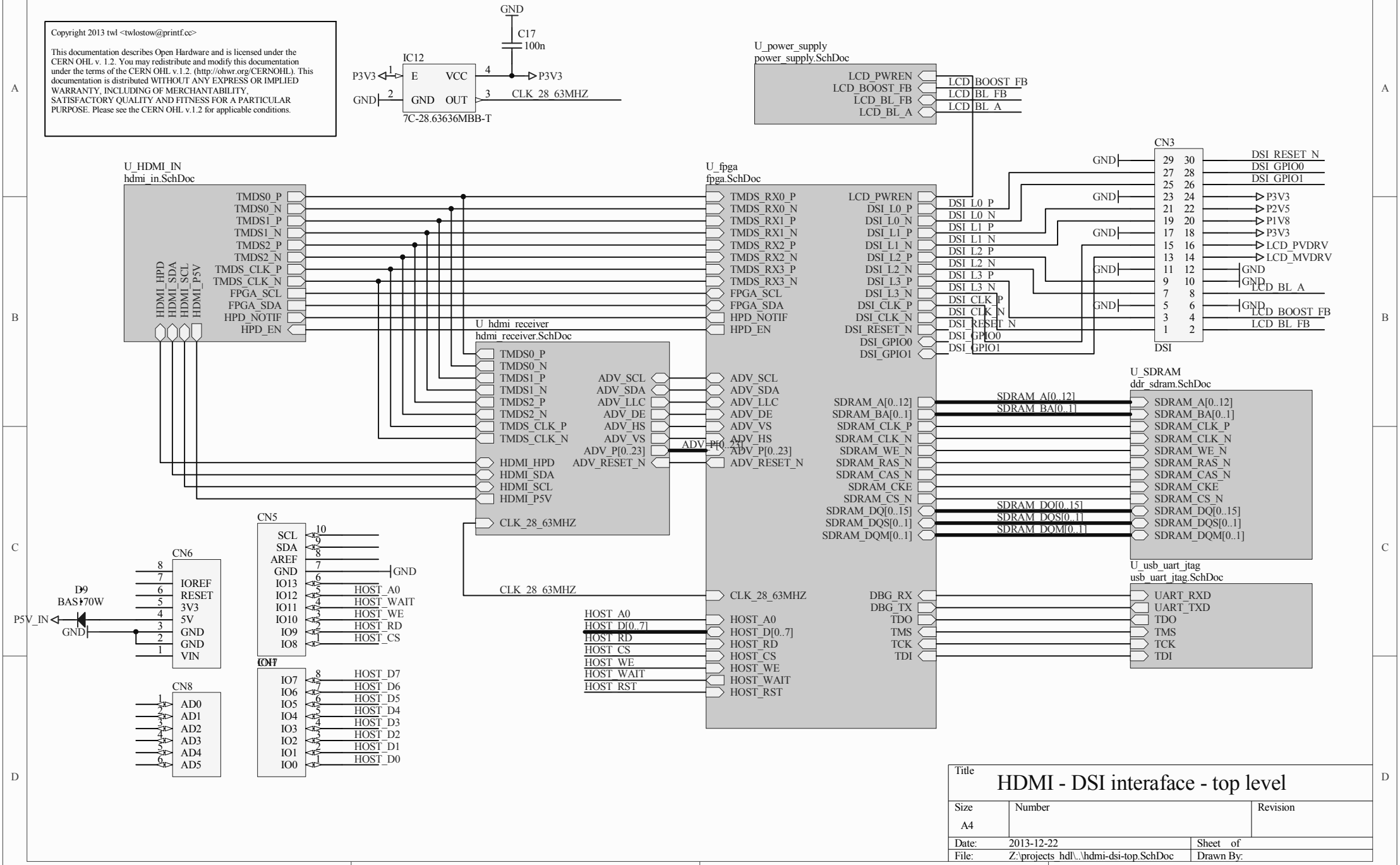
Title
Main FPGA
Size
A3
Number
Revision
Date:
2013-12-22
Sheet of
File:
Z:\projects_hdl\..\fpga.SchDoc
Drawn By:

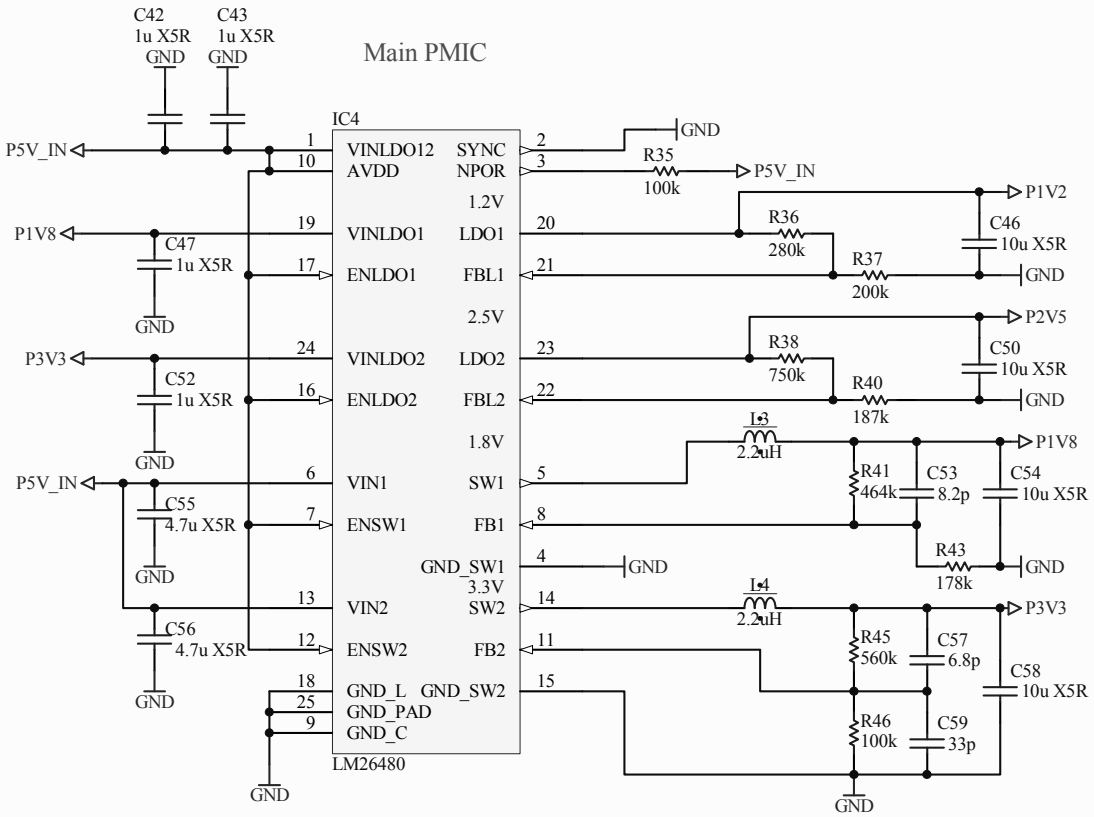


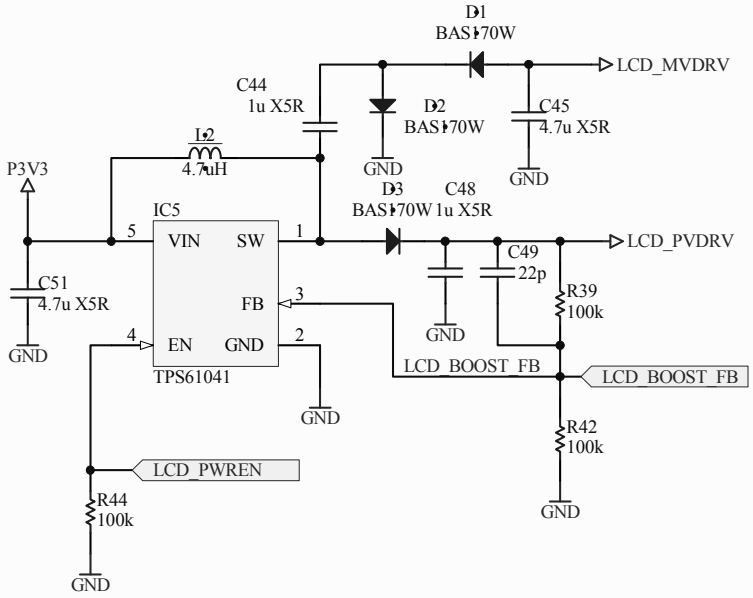
Title: Discrete HDMI receiver (ADV7611)

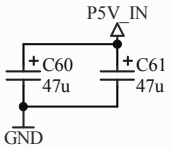
Size	Number	Revision
A4		
Date: 2013-12-22		Sheet of
File: Z:\projects_hdl\..\hdmi_receiver.SchDoc		Drawn By:

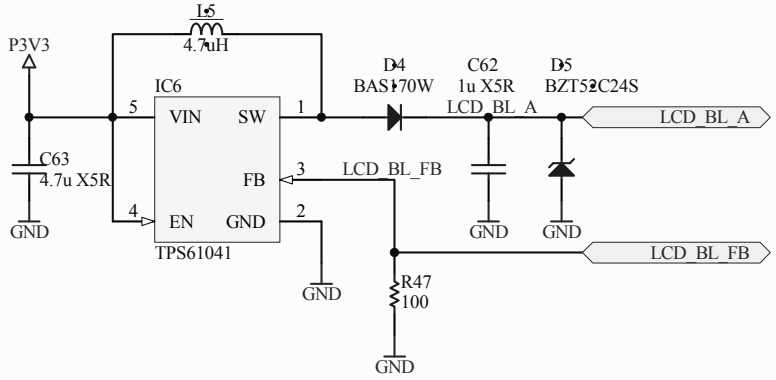


Title	HDMI - DSI interaface - top level	
Size: A4	Number:	Revision:
Date: 2013-12-22	Sheet of	
File: Z:\projects_hdl\..\hdmi-dsi-top.SchDoc	Drawn By:	

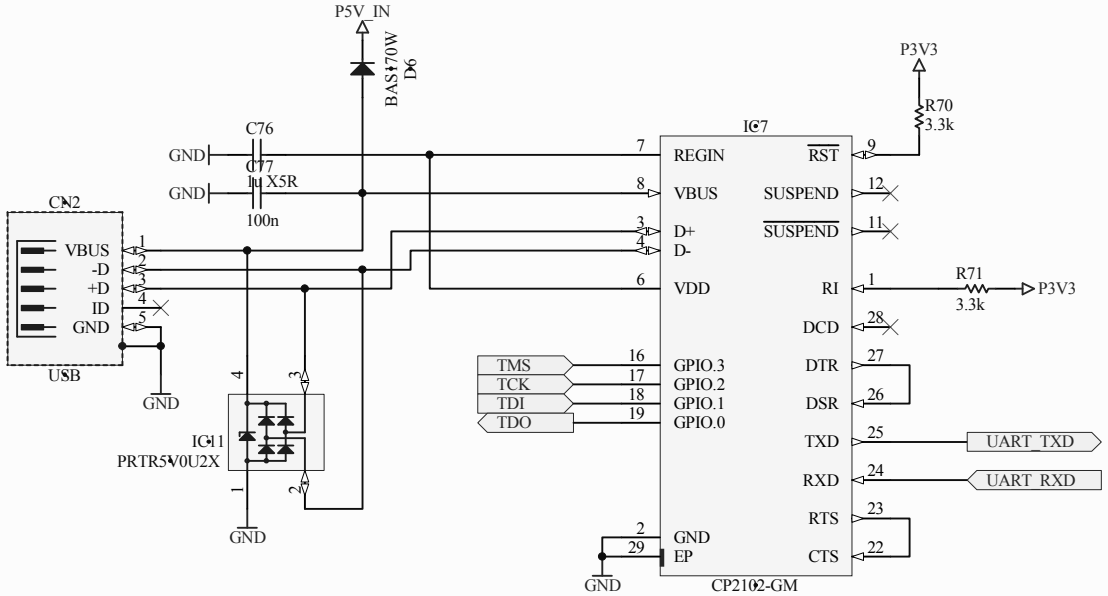








Title: Power supply		
Size: A	Number:	Revision:
Date: 2013-12-22		Sheet of
File: Z:\projects_hdl\..\power_supply.SchDoc		Drawn By:



Title	USB UART & JTAG	
Size: A4	Number:	Revision:
Date: 2013-12-22		Sheet of
File: Z:\projects_hdl\..\usb_uart_jtag.SchDoc		Drawn By: